R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2 and 13-15 under 35 U.S.C. §102(e) as being anticipated by Dujmenovic et al. (U.S. Patent No. 7,068,329; hereafter Dujmenovic) is respectfully traversed and should be withdrawn.

In contrast to Dujmenovic, the presently claimed invention (claim 1) provides an apparatus comprising (a) a first circuit configured to receive an encoded video signal at a first input and to present a decoded video signal at a first output and (b) a second circuit configured to receive the decoded video signal at a second input and to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where the first video output signal and the second video output signal are generated in response to the decoded video signal. Claims 13 and 14 include similar limitations.

The Office Action fails to meet the Office's burden to factually establish a *prima facie* case of anticipation. Specifically, Dujmenovic does not disclose or suggest (a) a first circuit configured to receive **an encoded video signal** (singular) at

a first input and to present **a decoded video signal** (singular) at a first output **and** (b) a second circuit configured to receive the decoded video signal at a second input and to present (i) **a first video output signal having a first resolution at a second output** and (ii) **a second video output signal having a second resolution at a third output** (plural video output signals and outputs), where the first video output signal and the second video output signal are generated in response to the decoded video signal (singular), as presently claimed. In particular, the video decoder 114 of Dujmenovic receives two separate video input signals, a first video signal on a first frequency and a second video signal on a second frequency, which are time division multiplexed by the tuner 110, at a single input (see FIGS. 1, 3 and 7 and column 1, line 55 through column 2, line 15 of Dujmenovic). The multiple video signals are decoded and stored in separate locations in the memory 116 of Dujmenovic (column 2, lines 27-42 of Dujmenovic). The display engine 118 of Dujmenovic combines the multiple images stored separately in the memory 116 to produce a single video output signal that is presented to a single display device 120 (column 2, lines 56-61 of Dujmenovic; also see page 4, section 4, lines 6-8 of the Office Action stating "Dujmenovic disclosed that multiple images (video signals) can be displayed simultaneously on a single display device").

A person of ordinary skill in the relevant art would not consider combining multiple decoded video channels, which were decoded from multiple input video signals, into a single video output signal, which is presented at a single output connected to a single display device as taught by Dujmenovic (see FIG. 1 and columns 1-2 of Dujmenovic) as being the same as (i) decoding a single video signal received at a single input (e.g., the step of (A) generating a decoded video signal in response to an encoded video signal, wherein the encoded video signal is received at a first input and the decoded video signal is presented at a first output, as presently claimed) and (ii) generating a plurality of video output signals at a plurality of outputs in response to the single decoded video signal (e.g., the steps of (B) generating (i) **a first video output signal** having a first resolution and (ii) **a second video output signal** having a second resolution in response to the decoded video signal and (C) presenting (i) the first video output signal at a first output and (ii) the second video output signal at a third output, as presently claimed). Therefore, Dujmenovic does not provide the factual support necessary for a *prima facie* case of anticipation. As such, the rejection does not appear to be sustainable and should be withdrawn.

Furthermore, the reference to CH1 and CH2 in the Office Action fails to clearly explain how and why the person of ordinary skill in the relevant art would find Dujmenovic to disclose or

suggest (i) **a first video output signal having a first resolution**, (ii) **a second video output signal having a second resolution**, (iii) **a second OUTPUT** at which the **first video output signal** is presented and (iv) **a third OUTPUT** at which the **second video output signal** is presented, as presently claimed (see section 2 on page 2 of the Office Action). Specifically, assuming, *arguendo*, the output of the video decoder 114 corresponds to the presently claimed first output (as suggested in lines 6-7 of section 2 on page 2 of the Office Action and for which Applicant's representative does not necessarily agree), the Office Action fails to explain where Dujmenovic discloses or suggests both (i) **a second output,** at which the first video output signal having the first resolution is presented, AND (ii) **a third output,** at which the second video output signal having the second resolution is presented, as presently claimed. The Office Action also fails to explain how Dujmenovic discloses or suggests the first video output signal having the first resolution and the second video output signal having the second resolution, as presently claimed, where CH1 and CH2 are shown in FIG. 1 of Dujmenovic as being in the same video signal and having the same size (see FIG. 1 of Dujmenovic and lines 8-13 in section 2 on page 2 of the Office Action). Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of anticipation. As such, the rejection is not sustainable and should be withdrawn.

Furthermore, assuming, *arguendo*, the items 116, 118 and 120 of Dujmenovic could be considered similar to the presently claimed second circuit (as suggested in lines 5-10 of section 2 on page 2 of the Office Action and for which Applicant's representative does not necessarily agree), Dujmenovic does not disclose or suggest a second circuit configured to receive the decoded video signal at a second input and to present (i) **a first video output signal having a first resolution at a second output** and (ii) **a second video output signal having a second resolution at a third output**, where the first video output signal and the second video output signal are generated in response to the decoded video signal, as presently claimed. Specifically, the video decoder 114 of Dujmenovic alternatively receives information from a first video signal and a second video signal and stores decoded information for the first video signal and the second video signal in separate locations in the memory 116 of Dujmenovic (see Abstract and column 1, lines 55 through column 2, line 42 of Dujmenovic). The display engine 118 of Dujmenovic combines the information for the first video signal and the second video signal from the separate locations in the memory 116 for display on a SINGLE monitor 120 connected to a SINGLE output of the display engine 118 (see FIG. 1 and column 2, lines 16-22 and lines 56-61 of Dujmenovic). In particular, Dujmenovic states:

> Fields associated with **a plurality of full motion video channels** are stored in memory 116 for retrieval by the display engine 118. When displayed upon **the display device 120**, multiple channels of video can be viewed. Generally, the multiple channels are displayed in separate windows where **a computer monitor** is being used (column 2, lines 56-61 of Dujmenovic, emphasis added by Applicant's representative).

Both of the terms "the display device 120" and "a computer monitor" used in Dujmenovic are singular. Dujmenovic is silent regarding the display engine 118 having more than one output. Furthermore, Dujmenovic is silent regarding **a first video OUTPUT SIGNAL having a first resolution** and **a second video OUTPUT SIGNAL having a second resolution**, as presently claimed. Therefore, Dujmenovic does not disclose or suggest each and every limitation of the presently claimed invention, arranged as in the claims. As such, the rejection does not appear to be sustainable and should be withdrawn.

Claims 2-12 and 15-25 depend, directly or indirectly, from either claim 1 or claim 14 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3-12 and 16-25 under 35 U.S.C. §103 as being unpatentable over Dujmenovic in view of Abe (U.S.

Patent No. 5,504,535) is respectfully traversed and should be withdrawn.

For the reasons present above, Dujmenovic does not teach or suggest each and every limitation of the presently claimed invention. Abe does not cure the deficiencies of Dujmenovic. Specifically, Abe does not teach or suggest a second circuit configured to receive a decoded video signal at a second input and to present (i) **a first video output signal having a first resolution at a second output** and (ii) **a second video output signal having a second resolution at a third output**, where the first video output signal and the second video output signal are generated in response to the decoded video signal, as presently claimed. Specifically, Abe shows two separate video INPUT SIGNALS. A first video input signal is described as an NTSC signal. The other video input signal is described as a MUSE encoded hi-vision signal (see FIG. 1 and column 7, line 34 through column 8, line 37 of Abe). Furthermore, Abe teaches combining the first video input signal and the second video input signal using an adding means 9 and presenting a **SINGLE VIDEO OUTPUT SIGNAL** to the CRT 20 (see FIG. 1 of Abe). Therefore, the combination of Dujmenovic and Abe does not provide the factual support necessary for a *prima facie* conclusion of obviousness. As such, the rejections do not appear to be sustainable and should be withdrawn.

Furthermore, the Office Action does not appear to meet the Office's burden with respect to establishing a motivation or suggestion to combine references. Specifically, the Office Action states:

> However, Dujmenovic disclosed that multiple images (video signals) can be displayed simultaneously on a single display device (see Fig. 1 item 120, col. 6, lines 8-9); . . . (page 4, section 4, lines 6-8 of the Office Action).

Since according to the Office Action Dujmenovic already discloses that multiple images can be displayed simultaneously on a single display device, there does not appear to be any motivation or suggestion for modifying Dujmenovic with Abe to "advantageously provide multiple images on a display simultaneously" as urged by the Office Action (see page 4, section 4, lines 11-16 of the Office Action. Therefore, the Office Action does not appear to have met the Office's burden of showing a motivation or suggestion for the combination of Dujmenovic and Abe to support a *prima facie* conclusion of obviousness. As such, the rejections do not appear to be sustainable and should be withdrawn.

Claims 3-12 and 16-25 depend, directly or indirectly, from either claim 1 or claim 14 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by he Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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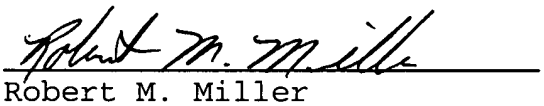

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